DEC 11 2002 \$

AMENDMENT TRANSMITTAL LETTER						Docket No. M4065.0014/P014 B	
Application No.		Filing Date		Examiner		Art Unit	
09/940,791		August 29, 2001 Kiesha L. Ro		se	2822		
Applicant(s): Lar	ry D. Kinsman				-	70	
nvention: LOW F	PROFILE BALL	. GRID ARRAY	/ PACKAGE			2822 DEC 13 700M	
TO THE COMMISSIONER FOR PATENTS						71/2	
Transmitted herewith is an amendment in the above-identified application.						Rogin	
The fee has been calculated and is transmitted as shown below.						3	
		CLAIM	S AS AMEN	DED			
	Claims Remaining After Amendment	Highest Number Previously Paid	Number Extra Claims Present	Rate			
Total Claims	7	- 20 =		х		0.00	
Independent Claims	3	- 3 =		x		0.00	
Multiple Depend	dent Claims (ch	eck if applicable	le)				
Other fee (pleas	se specify):					•	
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT:						0.00	
x Large Entity Small Entity							
x No additiona	al fee is require	d for this ame	ndment.	•			
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A check in t	he amount of \$		to cover	the filing fee is encl	osed.		
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X Charge any additional filing or application processing fees required under 37 CFR 1.16 and 1.17.

December 11, 2002

Dated:

Mark J. Thronson

Attorney Reg. No.: 33,082

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Docket No.: M4065.0014/P014-B (PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Larry D. Kinsman

Application No.: 09/940,791

Filed: August 29, 2001

For: LOW PROFILE BALL GRID ARRAY

PACKAGE

Group Art Unit: 2822

Examiner: Kiesha L. Rose

AMENDMENT UNDER 37 CFR § 1.116

ATTN: Box AF

Commissioner for Patents Washington, DC 20231

Dear Sir:

Responsive to the Office Action of September 11, 2002, finally rejecting claims 39-44, please amend the above-identified U.S. patent application as follows:

IN THE CLAIMS:

Please replace claims 39-44 with amended claims 39-44.

39. (twice amended) A processor system comprising:

a central processing unit; and

a memory device connected to said central processing unit, said memory device comprised of a plurality of low profile ball grid array semiconductor packages, said low profile ball grid array semiconductor packages comprised of a base substrate having a top surface and a bottom surface, with an aperture therein which extends from said top surface to said bottom surface,